In the Specification

Please delete the Paragraph beginning on lien 24 of Page 2 and replace this Paragraph with the following Paragraph.

--The aforementioned and other features are obtained according to the present invention, by measuring the number of transitions of the digital signal processing unit bus. The number of ~~transition~~ transitions is determined by coupling a conducting lead to each conductor of the digital signal processor bus. Each lead is coupled to an input terminal of a first latch/flip flop component. The output of the first latch/flip flop component is coupled to a first terminal of a logic "exclusive OR" gate and to an input of ~~the~~ a second latch flip flop component. The output terminal of the second latch/flip flop component is coupled to a second input terminal of the "exclusive OR" gate. The output terminal of the logic "exclusive OR" gate is coupled to a count unit, the count unit determining the number of transitions during each clock cycle. The count for each clock cycle is applied to an adder unit and the total number of counts determined. Because the transition on all of the bus conductors is monitored, the total number of transitions during a predetermined period can be determined. The total number of transitions determines the total energy consumption for a preselected period. The power consumed for an individual bus transitions can be determined by simulation or by other techniques. The power

consumed by the bus can be further divided into power consumed during the operation of the internal (on-chip) bus and the power consumed by the external (off-chip) bus. The power consumed can also be determined for one or more portions of a software program.- -